



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Khader S. Abdel-Hafez et al

Examiner R. Stephen Dildine, Jr.

Application No. 10/762,571

Art Unit 2133

Filed: January 23, 2004

For: Method and Apparatus for Debug, Diagnosis, and Yield

Improvement for Scan-Based Integrated Circuits

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed October 24, 2005, applicants hereby elect for the prosecution of this application:

Group I: Namely, Claims 1-33 and 50-66.

Applicants reserve the right to file one or more divisional applications directed to the nonelected claims, namely, Claims 34- 49 and 67-89.

Respectfully submitted,

Jim Zegeer, Reg. No. 18,957

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Date: November 3, 2005

In the event this paper is deemed not timely filed, the applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 26-0090 along with any other additional fees which may be required with respect to this paper.